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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/438,295	11/12/1999	KATSUKI HAZAMA	1737-013	9121

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EXAMINER	
HUA, LY	

ART UNIT	PAPER NUMBER
2135	9

DATE MAILED: 05/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/438,295	HAZAMA, KATSUKI	
	Examiner	Art Unit	
	Ly V. Hua	2135	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6,7,26-29,31 and 32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6,7,26-29,31 and 32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 08/931,519.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees.
   a. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993);
   b. *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985);
   c. *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982);
   d. *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and,
   e. *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

   A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

   Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 6, 7, 26-29, 31 and 32 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-31 of U.S. Patent No. 6,023,781. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following reasons.

   The subject matter claimed in the instant application is fully disclosed in the referenced copending application and would be covered by any patent granted on that copending application since the referenced copending application and the instant application are claiming common subject matter, as listed herein below:

   Furthermore, there is no apparent reason why applicant would be prevented from presenting claims corresponding to those of the instant application in the other copending application. See *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP ' 804.

   a. <u>As per claims 6 and 7:</u>
      i. Claim 6 claims a computer readable medium, which computer readable medium is:
         (1) storing program code
            (a) for causing a computer
               (i) to write
                  1) data of bits
                  2) in a semiconductor device
                     a) having a plurality of multilevel memory cells,
                     b) each cell storing at least three levels of data each,
         (2) comprising:
            (a) first program code means
               (i) for entering
                  1) at least
                     a) a first data composed of a plurality of first

data bits and
b) a second data composed of a plurality of second data bits,
i) the first and the second data having been coded by a coding method; and

(b) second program code means
(i) for arranging
1) the first and the second data bits
2) such that
a) at least
i) **a bit** of an N-order of the first data bits **and at least bit** of the M-order of the second data bits
ii) **are stored** in one of the cells, N and M being different integral numbers.

ii. With regard to claim 6:
(1) Claim 5 of patent number 6,023,781 substantially teaches the limitations as claimed in the present claim 7. Notice that the functions of the program code means in the present claim 6 are the steps performed by the method of claim 5 of the patent.
(2) However, claim 5 of the patent does not explicitly state that the steps are carried out by a computer as affected by program code means.
(3) It would have been obvious to a person having ordinary skill in the art at the time the invention was made to realize that operations done on a memory are perform by a computer according to a program instruction codes.

b. As per claim 7:
i. Claim 5 of patent number 6,023,781 substantially teaches the limitations as claimed in the present claim 7.

c. As per claim 26:
i. Claim 1 of patent number 6,023,781 substantially teaches the semiconductor device as claimed. Notice that the bit disperser (in the present claim) reads on the arranging means in claim 1 of the patent.

d. As per claim 27:
i. Claim 2 of patent number 6,023,781 teaches **controls the number of bits to be stored in at least one of the cells in accordance with capability of code error correction of the coding method**.

e. As per claim 28:
i. Claim 3 of patent number 6,023,781 substantially teaches the semiconductor device as claimed. Notice that the bit disperser's function of arranging (in the present claim) reads on the function of the arranging means in the claim of the patent.

f. As per claim 29:

i. Claim 29 claims that the semiconductor device according to claim 26, wherein the **multilevel memory cells are non-volatile semiconductor memories**.

ii. With regard to Claim 29:
(1) Claim 4 of patent number 6,023,781 claims that the multilevel memory cells are non-volatile semiconductor memories as claimed.

g. As per claims 31 and 32:
i. This claim has limitations that are similar to those of claim 6, and thus is similarly rejected with the same rationale applied against claim 6.

Claim Rejections - 35 USC ' 103

3. Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Baldi (5,761,222) in view of common practice in the art.

a. As per claim 32:
i. Claim 32 claims a computer readable medium
(1) storing program code
(2) for causing a computer to write
(a) at least one code data coded by a coding method
(b) in a semiconductor device
(i) having a plurality of multilevel memory cells, each cell storing one of at least three levels of data each,
(3) comprising
(a) the program code
(i) for dispersing
1) bits constituting the code data
2) over the plurality of multilevel memory cells.

ii. With regard to claim 32:
(1) Baldi (5,761,222) teaches [at col. 1, lines 49-53; col. 3, lines 7-9]
(a) dispersing [see Figure 3, 4, 5 or 6; (see also col. 3, lines 7-17, for the dispersion)]
(i) at least one code data [i.e., DI], [which code data has inherently been coded by certain coder according to certain coding method],
(ii) over cells in a semiconductor device [i.e., Figure 1] having
1) a plurality of multilevel memory cells [see Abstract, line 2; col. 1, lines 17, 64; col. 2, lines 2, 58-65], each of which cells storing one of at least three levels of data each [col. 2, lines 57-61],
(iii) [which writing is inherently done by a computer using Baldi's semiconductor device].
(2) However, Baldi does not explicitly teach:
(a) a program code which cause a computer to do such dispersing/writing.
(3) It would have been obvious to a person having ordinary skill in the art at the time the invention was made to:
(a) realize that the computer, in which Baldi=s a semiconductor device is used, would be controlled by a program code in order to do its operation in dispersing the code data bits.
(4) The skilled person would have been motivated to:
(a) realize this because it is a common knowledge in the art of writing/programming data bits into a memory requires a program code written to control a computer to do the writing/programming and which writing/programming would require the bits to be

distributed/dispersed/scattered/arranged so as to be stored/programmed/written into the cells of the memory.

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ly V. Hua whose telephone number is (703) 305-9684. The examiner can normally be reached on Monday to Friday, from 9:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vu Kim can be reached on (703) 305-4393. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

'Ly V. Hua
Primary Examiner
Art Unit 2135

L. Hua
May 8, 2003